

Express Mail Label No.: EV 292 459 643 US

Date of Deposit: February 25, 2004

10/786,357

<b>FORM PTO-1449/A and B (Modified)</b>  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>				APPLICATION NO.: Not Yet Assigned		ATTY. DOCKET NO.: A0312.70521US00	
				FILING DATE: <del>February</del> 2/25/04		CONFIRMATION NO.: Not Yet Assigned	
				APPLICANT: Brian D. Johansson et al.			
				GROUP ART UNIT: <del>Not Yet Assigned</del> 2816		EXAMINER: <del>Not Yet Assigned</del> Long nguyen	
Sheet	1	of	1				

## U.S. PATENT DOCUMENTS

Examiner's Initials	Cite No.	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication or of issue of Cited Document MM-DD-YYYY
		Number	Kind Code		
LN	A1	6,650,168	B1	Wang et al. 327/333	11/18/2003
LN	A2	6,556,061	B1	Chen et al. 327/333	04/29/2003
LN	A3	6,489,828	B1	Wang et al. 327/333	12/03/2002
LN	A4	6,414,534	B1	Wang et al. 327/333	07/02/2002

## FOREIGN PATENT DOCUMENTS

Examiner's Initials	Cite No.	Foreign Patent Document			Name of Patentee or Applicant of Cited Document (not necessary)	Date of Publication of Cited Document MM-DD-YYYY	Translation (Y/N)
		Office/ Country	Number	Kind Code			

## OTHER ART — NON PATENT LITERATURE DOCUMENTS

Examiner's Initials	Cite No	Include name of the author (in CAPITAL LETTERS) title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, relevant page(s), volume-issue number(s), publisher, city and/or country where published.	Translation (Y/N)	
LN	C1	Wen-Tai Wang et al., "Level Shifters for High-Speed 1-V to 3.3 V Interfaces in a 0/13- $\mu$ m Cu-Interconnection/Low-k CMOS Technology; pp. 307-310, 2001 IEEE;		
LN	C2	Texas Instruments Translation Overview; pp. 1-4, 2003;		
LN	C3	"Voltage Level Translating Circuit", Oct. 1959, IBM Technical Disclosure Bulletin;		
LN	C4	"Voltage Level Translation Circuit", June 1975, pp. 1-2, IBM Technical Disclosure Bulletin;		
LN	C5	Charles D. Rakes, "Circuit Circus", pp. 59-62; March 1999, Popular Electronics;		
LN	C6	"Cascaded Common-Gate FET IC Provides Flexible Level Translation", Electronic Design, pp. 1 of 5; 2/3/04		

EXAMINER	Long nguyen	DATE CONSIDERED	10/14/05
----------	-------------	-----------------	----------